# CLAIMS

What is claimed is:

1. An architecture for a data storage device, comprising:

a first data storage device control circuit that includes a first input/output (I/O) interface; and

an application circuit including a buffer that stores application data and data storage device control data, a mapping driver that maps logical addresses to physical addresses, and a second I/O interface that communicates with at least one of said buffer and said mapping driver, wherein said physical addresses and data are transmitted by said second I/O interface to said first I/O interface.

2. The data storage device architecture of claim 1 wherein said first data storage device control circuit is implemented on a data storage device assembly (DSDA) printed circuit board (PCB).

3. The data storage device architecture of claim 1 wherein said first data storage device control circuit includes a data storage device controller (DSDC), a data storage device processor, a spindle motor driver, a read/write arm driver, and a read channel driver, wherein said DSDC communicates with said first I/O interface and with at least one of said data storage device processor, said spindle motor driver, said read/write arm driver, and said read channel driver.

4. The data storage device architecture of claim 3 wherein said application circuit includes at least one of an application specific integrated circuit (ASIC) and an application processor that communicates with said buffer.

5. The data storage device architecture of claim 3 further comprising a data storage device that includes:

a data storage device platter;

a read/write arm;

a read/write head arranged on said read/write arm;

a spindle motor that communicates with said spindle motor driver and that rotates said data storage device platter;

a read/write arm actuator that communicates with said read/write arm driver and that adjusts a position of said read/write arm; and

a preamp circuit that communicates with said read channel driver and said read/write head.

6. The data storage device architecture of claim 1 wherein said mapping driver at least one of maps logical addresses to physical addresses and monitors a location of a read/write head of a data storage device.

7. The data storage device architecture of claim 1 wherein said first and second I/O interfaces are serial ATA interfaces.

8. The data storage device architecture of claim 1 wherein said first and second I/O interfaces are parallel interfaces.

9. The data storage device architecture of claim 4 wherein at least two of said application processor, said ASIC, said buffer, and said second I/O interface are implemented by a first integrated circuit.

10. The data storage device architecture of claim 4 wherein said first data storage device control circuit includes a first security module that communicates with said data storage device processor and said application circuit includes a second security module that communicates with said application processor, and wherein said first and second security modules implement a security protocol.

11. The data storage device architecture of claim 1 wherein said application circuit includes a port multiplier.

12. The data storage device architecture of claim 3 wherein at least two of said data storage device processor, said DSDC, said spindle motor driver, said read/write arm driver, said first I/O interface and said read channel driver are implemented by a second integrated circuit.

13. The data storage device architecture of claim 4 wherein at least one of said application processor and said ASIC sends a data request that includes an expiration time to said mapping driver, and wherein said mapping driver cancels said data request if said DSDC does not respond to said data request before said expiration time.

14. The data storage device architecture of claim 4 wherein at least one of said application processor and said ASIC sends a data request to said mapping driver, wherein said mapping driver periodically receives at least one of head location and sector location status from said DSDC, and wherein said mapping driver sends an estimated response time for said data request to said at least one of said application processor and said ASIC.

15. The data storage device architecture of claim 14 wherein said at least one of said application processor and said ASIC schedules at least one task that is not data access related before said estimated response time elapses.

16. The data storage device architecture of claim 1 wherein said application circuit is implemented on an application printed circuit board (PCB).

17. The data storage device architecture of claim 11 further comprising a plurality of second data storage device control circuits each including a third I/O interface, wherein said port multiplier communicates with said third I/O interface of said second data storage device control circuits.

18. An application circuit for a data storage device including a read/write head, comprising:

at least one of an application processor and an application specific integrated circuit (ASIC);

a buffer that communicates with said at least one of said application processor and said ASIC and that stores data storage device control related data and application related data;

a mapping driver that communicates with said buffer and that at least one of maps logical addresses to physical addresses and monitors a location of the read/write head; and

a first I/O interface that communicates with at least one of said mapping driver, said application processor, said ASIC, and said buffer.

19. The application circuit of claim 18 further comprising a data storage device controller (DSDC) that communicates with said mapping driver wherein said first I/O interface transmits data storage device control data including at least one of arm position data and spindle control data to a data storage device control circuit.

20. The application circuit of claim 18 wherein said application processor performs both data storage device control related processing and application related processing.

21. The application circuit of claim 18 wherein said first I/O interface transmits physical addresses and data to a data storage device control circuit.

22. The application circuit of claim 18 wherein said ASIC communicates with at least one of said application processor and said buffer.

23. The application circuit of claim 18 wherein said first I/O interface is a serial ATA interface.

24. The application circuit of claim 18 wherein said first I/O interface is a parallel interface.

25. The application circuit of claim 18 wherein at least two of said application processor, said ASIC, said buffer, and said first I/O interface are implemented by a first integrated circuit.

26. The application circuit of claim 21 wherein said application circuit includes a port multiplier.

27. The application circuit of claim 18 further comprising a security module that communicates with said application processor and that implements a security protocol.

28. The application circuit of claim 18 wherein said application circuit is implemented on an application printed circuit board (PCB).

29. The application circuit of claim 26 wherein said application circuit communicates with a plurality of second data storage device control circuits each including a third I/O interface, and wherein said port multiplier communicates with said third I/O interface of said second data storage device control circuits.

30. A data storage device control circuit for a data storage device, comprising:

a data storage device processor;

a data storage device controller (DSDC) that communicates with said data storage device processor;

at least one of a spindle motor driver, a read/write arm driver, and a read channel driver that communicates with said DSDC; and

a first input/output (I/O) interface that receives data to be stored on the data storage device and physical address data from an external I/O interface, wherein said DSDC uses said physical address data to store said data on the data storage device.

31. The data storage device control circuit of claim 30 wherein said data storage device control circuit is implemented on a data storage device assembly (DSDA) printed circuit board (PCB).

32. The data storage device control circuit of claim 30 wherein said external I/O interface communicates with an external mapping driver and said first I/O interface.

33. The data storage device control circuit of claim 32 wherein said first and external interfaces are serial ATA interfaces.

34. The data storage device control circuit of claim 32 wherein said first and external interfaces are parallel interfaces.

35. The data storage device control circuit of claim 30 further comprising a security module that communicates with said data storage device processor and that implements a security protocol.

36. The data storage device control circuit of claim 30 wherein at least two of said data storage device processor, said DSDC, said spindle motor driver, said read/write arm driver, said read channel driver, and said first input/output (I/O) interface are implemented by an integrated circuit.

37. A data storage device control circuit for a data storage device that interfaces with an application circuit including a second input/output (I/O) interface, comprising:

a first input/output interface that receives data to be stored on the data storage device and data storage device control data including at least one of arm position data and spindle control data from the second I/O interface; and

at least one of a spindle motor driver, a read/write arm driver, and a read channel driver that communicates with said first I/O interface.

38. The data storage device control circuit of claim 37 wherein said data storage device control circuit is implemented on a data storage device assembly (DSDA) printed circuit board (PCB).

39. The data storage device control circuit of claim 37 wherein the second I/O interface communicates with said DSDC, said external mapping driver and said first I/O interface.

40. The data storage device control circuit of claim 39 wherein said first and second interfaces are serial ATA interfaces.

41. The data storage device control circuit of claim 39 wherein said first and second interfaces are parallel interfaces.

42. The data storage device control circuit of claim 37 wherein at least two of said spindle motor driver, said read/write arm driver, said read channel driver, and said first input/output (I/O) interface are implemented by an integrated circuit.

43. An architecture for a data storage device, comprising:

a data storage device control circuit that includes a first input/output (I/O) interface; and

an application circuit including a buffer that stores application data and data storage device control data, a mapping driver that maps logical addresses to physical addresses, a data storage device controller (DSDC), and a second I/O interface that communicates with at least one of said DSDC, said mapping driver and said buffer, wherein data to be stored on the data storage device and data storage device control signals including at least one of read/write arm position data and spindle control data are transmitted by said second I/O interface to said first I/O interface.

44. The data storage device architecture of claim 43 wherein said data storage device control circuit includes at least one of a spindle motor driver, a read/write arm driver, and a read channel driver that communicate with said first I/O interface.

45. The data storage device architecture of claim 44 wherein said application circuit includes at least one of an application specific integrated circuit (ASIC) and an application processor that communicates with said buffer.

46. The data storage device architecture of claim 43 wherein said data storage device control circuit is implemented on a data storage device assembly (DSDA) printed circuit board (PCB).

47. The data storage device architecture of claim 44 further comprising a data storage device that includes:

a data storage device platter;

a read/write arm;

a read/write head arranged on said read/write arm;

a spindle motor that communicates with said spindle motor driver and that rotates said data storage device platter;

a read/write arm actuator that communicates with said read/write arm driver and that adjusts a position of said read/write arm; and

a preamp circuit that communicates with said read channel driver and said read/write head.

48. The data storage device architecture of claim 43 wherein said mapping driver at least one of maps logical addresses to physical addresses and monitors a location of a read/write head of a data storage device.

49. The data storage device architecture of claim 43 wherein said first and second I/O interfaces are serial ATA interfaces.

50. The data storage device architecture of claim 43 wherein said first and second I/O interfaces are parallel interfaces.

51. The data storage device architecture of claim 45 wherein at least two of said application processor, said ASIC, said buffer, said DSDC, said mapping driver and said second I/O interface are implemented by a first integrated circuit.

52. The data storage device architecture of claim 43 wherein said application circuit includes a port multiplier.

53. The data storage device architecture of claim 43 wherein at least two of said spindle motor driver, said read/write arm driver, said read channel driver and said I/O interface are implemented by a second integrated circuit.

54. The data storage device architecture of claim 45 wherein at least one of said application processor and said ASIC sends a data request that includes an expiration time to said mapping driver, and wherein said mapping driver cancels said data request if said DSDC does not respond to said data request before said expiration time.

55. The data storage device architecture of claim 45 wherein at least one of said application processor and said ASIC sends a data request to said mapping driver, wherein said mapping driver periodically receives at least one of head location and sector location status from said DSDC, and wherein said mapping driver sends an estimated response time for said data request to said at least one of said application processor and said ASIC.

56. The data storage device architecture of claim 55 wherein said at least one of said application processor and said ASIC schedules at least one task that is not data access related before said estimated response time elapses.

57. The data storage device architecture of claim 43 wherein said application circuit is implemented on an application printed circuit board (PCB).

58. The data storage device architecture of claim 52 further comprising a plurality of second data storage device control circuits each including a third I/O interface, wherein said port multiplier communicates with said third I/O interface of said second data storage device control circuits.

59. The data storage device architecture of claim 44 wherein at least two of said spindle motor driver, said read/write arm driver, said read channel driver and said first I/O interface are implemented by an integrated circuit.

60. An architecture for a data storage device, comprising:

first control means for controlling the data storage device and that includes first interface means for providing an input/output interface for said first control means; and

application means for providing application functionality and including buffer means for storing application data and data storage device control data, mapping means for mapping logical addresses to physical addresses, and second interface means for providing an input/output interface for said application means and for communicating with at least one of said buffer means and said mapping means, wherein said physical addresses and data are transmitted by said second interface means to said first interface means.

61. The data storage device architecture of claim 60 wherein said first control means is implemented on a data storage device assembly (DSDA) printed circuit board (PCB).

62. The data storage device architecture of claim 60 wherein said first control means includes data storage device controller (DSDC) means for providing data storage device controller functions, data storage device processing means for performing data storage device processing functions, and driving means for providing at least one of a spindle motor driver, a read/write arm driver, and a read channel driver, wherein said DSDC means communicates with said first interface means and with at least one of said data storage device processing means and said driving means.

63. The data storage device architecture of claim 62 wherein said application means includes application processing means for performing application processing and for communicating with said buffer means.

64. The data storage device architecture of claim 62 further comprising a data storage device, wherein said data storage device includes:

a data storage device platter;

a read/write arm;

a read/write head arranged on said read/write arm;

a spindle motor that communicates with said spindle motor driver and that rotates said data storage device platter;

a read/write arm actuator that communicates with said read/write arm driver and that adjusts a position of said read/write arm; and

a preamp circuit that communicates with said read channel driver and said read/write head.

65. The data storage device architecture of claim 60 wherein said mapping means at least one of maps logical addresses to physical addresses and monitors a location of a read/write head of a data storage device.

66. The data storage device architecture of claim 60 wherein said first and second interface means are serial ATA interfaces.

67. The data storage device architecture of claim 60 wherein said first and second interface means are parallel interfaces.

68. The data storage device architecture of claim 63 wherein at least two of said application processing means, said buffer means, and said second interface means are implemented by a first integrated circuit.

69. The data storage device architecture of claim 63 wherein said first control means includes first security means for communicating with said data storage device processing means and said application means includes second security means for communicating with said application processing means, said first and second security means for implementing a security protocol.

70. The data storage device architecture of claim 60 wherein said application means includes port multiplying means for communicating with multiple ports.

71. The data storage device architecture of claim 62 wherein at least two of said data storage device processing means, said DSDC means, said driving means, and said first interface means are implemented by a second integrated circuit.

72. The data storage device architecture of claim 63 wherein said application processing means sends a data request that includes an expiration time to said mapping means, and wherein said mapping means cancels said data request if said DSDC means does not respond to said data request before said expiration time.

73. The data storage device architecture of claim 63 wherein said application processing means sends a data request to said mapping means, wherein said mapping means periodically receives at least one of head location and sector location status from said DSDC means, and wherein said mapping means sends an estimated response time for said data request to said application processing means.

74. The data storage device architecture of claim 73 wherein said application processing means schedules at least one task that is not data access related before said estimated response time elapses.

75. The data storage device architecture of claim 60 wherein said application means is implemented on an application printed circuit board (PCB).

76. The data storage device architecture of claim 70 further comprising a plurality of second control means for controlling additional data storage devices each including third interface means for providing an input/output interface, wherein said port multiplying means communicates with said third interface means of said second control means.

77. An application circuit for a data storage device including a read/write head, comprising:

application processing means for performing application processing functions;

buffer means that communicates with said application processing means for storing data storage device control related data and application related data;

mapping means that communicates with said buffer means for at least one of mapping logical addresses to physical addresses and monitoring a location of the read/write head; and

first interface means for providing an input/output interface for said application processing means and for communicating with at least one of said mapping means, said application processing means, and said buffer means.

78. The application circuit of claim 77 further comprising data storage device controller (DSDC) means for providing data storage device controller functions and for communicating with said mapping means, wherein said first interface means transmits data storage device control data including at least one of arm position data and spindle control data to a first control means for controlling a data storage device.

79. The application circuit of claim 77 wherein said application processing means performs both data storage device control related processing and application related processing.

80. The application circuit of claim 77 wherein said first interface means transmits physical addresses and data to a first control means for controlling a data storage device.

81. The application circuit of claim 77 further comprising an application specific integrated circuit (ASIC) that communicates with at least one of said application processing means and said buffer means.

82. The application circuit of claim 77 wherein said first interface means is a serial ATA interface.

83. The application circuit of claim 77 wherein said first interface means is a parallel interface.

84. The application circuit of claim 77 wherein at least two of said application processing means, said buffer means, and said first interface means are implemented by a first integrated circuit.

85. The application circuit of claim 80 wherein said application means includes port multiplying means for communicating with multiple ports.

86. The application circuit of claim 77 further comprising security means that communicates with said application processing means for implementing a security protocol.

87. The application circuit of claim 77 wherein said application means is implemented on an application printed circuit board (PCB).

88. The application circuit of claim 85 wherein said application means communicates with a plurality of second control means for controlling additional data storage devices each including third interface means for providing an input/output interface, and wherein said port multiplying means communicates with said third interface means of said second control means.

89. A data storage device control circuit for a data storage device, comprising:

data storage device processing means for performing data storage device processing functions;

data storage device controller (DSDC) means for communicating with said data storage device processing means and for performing data storage device controller functions;

driving means for providing at least one of a spindle motor driver, a read/write arm driver, and a read channel driver and for communicating with said DSDC means; and

first interface means for providing an input/output interface for said data storage device control circuit and for receiving data to be stored on the data storage device and physical address data, wherein said DSDC means uses said physical address data to store said data on the data storage device.

90. The data storage device control circuit of claim 89 wherein said data storage device control means is implemented on a data storage device assembly (DSDA) printed circuit board (PCB).

91. The data storage device control circuit of claim 89 further comprising:

external interface means for communicating with said first interface means; and

external mapping means for mapping logical addresses to physical addresses and for communicating with said external interface means.

92. The data storage device control circuit of claim 91 wherein said first and external interface means are serial ATA interfaces.

93. The data storage device control circuit of claim 91 wherein said first and external interface means are parallel interfaces.

94. The data storage device control circuit of claim 89 further comprising security means that communicates with said data storage device processing means for implementing a security protocol.

95. The data storage device control circuit of claim 89 wherein at least two of said data storage device processing means, said DSDC means, said driving means, and said first interface means are implemented by an integrated circuit.

96. A data storage device control circuit for a data storage device that interfaces with an application circuit including a first input/output (I/O) interface, comprising:

second interface means for providing an input/output interface for said data storage device control circuit and for receiving data to be stored on the data storage device and data storage device control data including at least one of arm position data and spindle control data from the second I/O interface; and

driving means for providing at least one of a spindle motor driver, a read/write arm driver, and a read channel driver and for communicating with said first interface means.

97. The data storage device control circuit of claim 96 wherein said data storage device control circuit is implemented on a data storage device assembly (DSDA) printed circuit board (PCB).

98. The data storage device control circuit of claim 96 wherein the second interface means communicates with said DSDC means, said external mapping means and said first interface means.

99. The data storage device control circuit of claim 98 wherein said first and second interface means are serial ATA interfaces.

100. The data storage device control circuit of claim 98 wherein said first and second interface means are parallel interfaces.

101. The data storage device control circuit of claim 96 wherein said driving means and said second interface means are implemented by an integrated circuit.

102. An architecture for a data storage device, comprising:

first control means for controlling the data storage device and that includes first interface means for providing an input/output interface for said first control means; and

application means including buffer means for storing application data and data storage device control data, mapping means for mapping logical addresses to physical addresses, data storage device controller (DSDC) means for providing data storage device controller functions, and second interface means for providing an input/output interface for said application means and for communicating with at least one of said DSDC means, said mapping means and said buffer means, wherein data to be stored on the data storage device and data storage device control signals including at least one of read/write arm position data and spindle control data are transmitted by said second interface means to said first interface means.

103. The data storage device architecture of claim 102 wherein said first control means includes driving means for providing at least one of a spindle motor driver, a read/write arm driver, and a read channel driver that communicates with said first interface means.

104. The data storage device architecture of claim 103 wherein said application means includes application processing means for performing application processing functions and for communicating with said buffer means.

105. The data storage device architecture of claim 102 wherein said first control means is implemented on a data storage device assembly (DSDA) printed circuit board (PCB).

106. The data storage device architecture of claim 103 further comprising a data storage device that includes:

a data storage device platter;

a read/write arm;

a read/write head arranged on said read/write arm;

a spindle motor that communicates with said spindle motor driver and that rotates said data storage device platter;

a read/write arm actuator that communicates with said read/write arm driver and that adjusts a position of said read/write arm; and

a preamp circuit that communicates with said read channel driver and said read/write head.

107. The data storage device architecture of claim 102 wherein said mapping means at least one of maps logical addresses to physical addresses and monitors a location of a read/write head of a data storage device.

108. The data storage device architecture of claim 102 wherein said first and second interface means are serial ATA interfaces.

109. The data storage device architecture of claim 102 wherein said first and second interface means are parallel interfaces.

110. The data storage device architecture of claim 104 wherein at least two of said application processing means, said ASIC, said buffer means, said DSDC means, said mapping means and said second interface means are implemented by a first integrated circuit.

111. The data storage device architecture of claim 102 wherein said application means includes port multiplying means for communicating with multiple ports.

112. The data storage device architecture of claim 102 wherein said driving means and said interface means are implemented by a second integrated circuit.

113. The data storage device architecture of claim 104 wherein said application processing means sends a data request that includes an expiration time to said mapping means, and wherein said mapping means cancels said data request if said DSDC means does not respond to said data request before said expiration time.

114. The data storage device architecture of claim 104 wherein said application processing means sends a data request to said mapping means, wherein said mapping means periodically receives at least one of head location and sector location status from said DSDC means, and wherein said mapping means sends an estimated response time for said data request to said application processing means.

115. The data storage device architecture of claim 114 wherein said application processing means schedules at least one task that is not data access related before said estimated response time elapses.

116. The data storage device architecture of claim 102 wherein said application means is implemented on an application printed circuit board (PCB).

117. The data storage device architecture of claim 111 further comprising a plurality second control means for controlling additional data storage devices each including third interface means for providing an input/output interface, wherein said port multiplying means communicates with said third interface means of said second control means.

118. The data storage device architecture of claim 103 wherein said driving means and said first interface means are implemented by an integrated circuit.

119. A method for operating a data storage device, comprising:

storing application data and data storage device control data in a buffer associated with an application circuit;

mapping logical addresses to physical addresses using said application circuit; and

transmitting said physical addresses and data from said application circuit to a data storage device circuit.

120. The method of claim 119 further comprising implementing said data storage device control circuit on a data storage device assembly (DSDA) printed circuit board (PCB).

121. The method of claim 119 further comprising at least one of mapping logical addresses to physical addresses and monitoring a location of a read/write head of a data storage device.

122. The method of claim 119 wherein said data storage device control circuit and said application circuit communicate using a serial ATA interface.

123. The method of claim 119 wherein said data storage device control circuit and said application circuit communicate using a parallel interface.

124. The method of claim 119 further comprising implementing a security protocol between said data storage device control circuit and said application circuit.

125. The method of claim 119 further comprising:

sending a data request using said application circuit that includes an expiration time; and

canceling said data request using said application circuit if a response to said data request does not occur before said expiration time.

126. The method of claim 119 further comprising:

sending a data request using said application circuit;

periodically receiving at least one of head location and sector location status data from said data storage device control circuit;

estimating a response time for said data request from said head location and sector location status data .

127. The method of claim 126 further comprising scheduling at least one task that is not data access related before said estimated response time elapses.

128. The method of claim 119 wherein said application circuit is implemented on an application printed circuit board (PCB).

129. The method of claim 119 further comprising using a port multiplier to communicate with a plurality of second data storage device control circuits.

130. A method for operating an application circuit for a data storage device including a read/write head, comprising:

storing data storage device control related data and application related data in memory associated with an application circuit; and

at least one of mapping logical addresses to physical addresses and monitoring a location of the read/write head using said application circuit.

131. The method of claim 130 further comprising transmitting data storage device control data including at least one of arm position data and spindle control data from said application circuit to a data storage device control circuit.

132. The method of claim 130 further comprising performing both data storage device control related processing and application related processing using said application circuit.

133. The method of claim 130 further comprising transmitting physical addresses and data from said application circuit to a data storage device control circuit.

134. The method of claim 133 further comprising providing a serial ATA interface between said application circuit and said data storage device control circuit.

135. The method of claim 133 further comprising providing a parallel interface between said application circuit and said data storage device control circuit.

136. The method of claim 130 wherein said application circuit is implemented by a first integrated circuit.

137. The method of claim 133 further comprising implementing a security protocol between said application circuit and said data storage device control circuit.

138. The method of claim 133 wherein said application circuit is implemented on an application printed circuit board (PCB).

139. The method of claim 133 further comprising using a port multiplier to communicate with a plurality of second data storage device control circuits.

140. A method for operating a data storage device control circuit for a data storage device, comprising:

transmitting data to be stored on the data storage device from an application circuit to said data storage device control circuit;

transmitting physical address data from an application circuit to said data storage device control circuit; and

using said physical address data at said data storage device control circuit to store said data on the data storage device.

141. The method of claim 140 wherein said data storage device control circuit is implemented on a data storage device assembly (DSDA) printed circuit board (PCB).

142. The method of claim 140 further comprising using a serial ATA interface for communications between said data storage device control circuit and said application circuit.

143. The method of claim 140 further comprising using a parallel interface for communications between said data storage device control circuit and said application circuit.

144. The method of claim 140 further comprising implementing a security protocol between said application circuit and said data storage device control circuit.

145. The method of claim 140 further comprising implementing said data storage device control circuit using an integrated circuit.

146. A method for operating a data storage device control circuit for a data storage device that interfaces with an application circuit, comprising:

receiving data to be stored on the data storage device from the application circuit at said data storage device control circuit; and

receiving data storage device control data including at least one of arm position data and spindle control data from the application circuit at said data storage device control circuit.

147. The method of claim 146 wherein said data storage device control circuit is implemented on a data storage device assembly (DSDA) printed circuit board (PCB).

148. The method of claim 146 further comprising using a serial ATA interface for communications between said data storage device control circuit and said application circuit.

149. The method of claim 146 further comprising using a parallel interface for communications between said data storage device control circuit and said application circuit.

150. The method of claim 146 further comprising implementing said data storage device control circuit using an integrated circuit.

151. A method for providing an architecture for a data storage device, comprising:

storing application data and data storage device control data in an application circuit;

mapping logical addresses to physical addresses using said application circuit;

transmitting data to be stored on the data storage device from said application circuit to said data storage device control circuit; and

transmitting data storage device control signals including at least one of read/write arm position data and spindle control data from said application circuit to said data storage device control circuit.

152. The method of claim 151 further comprising implementing said data storage device control circuit on a data storage device assembly (DSDA) printed circuit board (PCB).

153. The method of claim 151 further comprising at least one of mapping logical addresses to physical addresses and monitoring a location of a read/write head of a data storage device.

154. The method of claim 151 further comprising using a serial ATA interface for communications between said data storage device control circuit and said application circuit.

155. The method of claim 151 further comprising using a parallel interface for communications between said data storage device control circuit and said application circuit.

156. The method of claim 151 further comprising implementing said application circuit using a first integrated circuit.

157. The method of claim 151 further comprising implementing said data storage device control circuit using a second integrated circuit.

158. The method of claim 151 further comprising:

sending a data request that includes an expiration time using said application circuit; and

canceling said data request if a response to said data request does not occur before said expiration time.

159. The method of claim 151 further comprising:

generating a data request using said application circuit;

periodically monitoring at least one of head location and sector location status using said application circuit; and

generating an estimated response time for said data request.

160. The method of claim 159 further comprising scheduling at least one task that is not data access related before said estimated response time elapses.

161. The method of claim 151 wherein said application circuit is implemented on an application printed circuit board (PCB).

162. The method of claim 151 further comprising using a port multiplier associated with said application circuit to communicate with a plurality of second data storage device control circuits.

163. The method of claim 151 wherein said data storage device control circuit is implemented by an integrated circuit.

164. A processor chipset that communicates with a data storage device, comprising:

an input/output (I/O) circuit that provides an I/O interface for at least one of serial, audio, basic input/output system (BIOS), local area network, mouse, and keyboard connections and that includes:

a mapping driver that maps logical addresses to physical addresses;

a data storage device controller (DSDC) that communicates with said mapping driver and that controls the data storage device; and

a first I/O interface that communicates with at least one of said DSDC and said mapping driver, wherein data to be stored on the data storage device and data storage device control signals including at least one of read/write arm position data and spindle control data are transmitted by said first I/O interface to the data storage device.

165. The processor chipset of Claim 164 further comprising a processor that performs at least one of data and control processing and that communicates with said I/O circuit.

166. The processor chipset of Claim 165 further comprising:

a system bus that transfers data and that communicates with said processor;

a peripheral component interconnect (PCI) bus that communicates with said processor and that provides an interface to an expansion card slot; and

a Northbridge chipset that communicates with said processor over said system bus,

wherein said I/O circuit is implemented by a Southbridge chipset that communicates with said PCI bus.

167. The processor chipset of Claim 164 wherein said processor chipset communicates with a data storage device control circuit that includes a second I/O interface and at least one of a spindle motor driver, a read/write arm driver, and a read channel driver, and wherein said first I/O interface communicates with said second I/O interface.

168. The processor chipset of Claim 167 wherein at least one of said DSDC and said mapping driver communicates data and control information to said read channel in-band over a serial link.

169. The processor chipset of Claim 167 wherein at least one of said DSDC and said mapping driver communicates data to said read channel in-band and control information to said read channel out-of-band.

170. The processor chipset of Claim 167 wherein the data storage device includes:

a data storage device platter;

a read/write arm;

a read/write head arranged on said read/write arm;

a spindle motor that communicates with said spindle motor driver and that rotates said data storage device platter;

a read/write arm actuator that communicates with said read/write arm driver and that adjusts a position of said read/write arm; and

a preamp circuit that communicates with said read channel driver and said read/write head.

171. The processor chipset of Claim 164 wherein said mapping driver at least one of maps logical addresses to physical addresses and monitors a location of a read/write head of the data storage device.

172. The processor chipset of Claim 167 wherein said first and second I/O interfaces are serial ATA interfaces.

173. The processor chipset of Claim 164 wherein said I/O circuit includes a port multiplier that communicates with said first I/O interface.

174. The processor chipset of Claim 165 wherein said processor sends a data request that includes an expiration time to said mapping driver, and wherein said mapping driver cancels said data request if said DSDC does not respond to said data request before said expiration time.

175. The processor chipset of Claim 165 wherein said processor sends a data request to said mapping driver, wherein said mapping driver periodically receives at least one of head location and sector location status from said DSDC, and wherein said mapping driver sends an estimated response time for said data request to said processor.

176. The processor chipset of Claim 175 wherein said processor schedules at least one task that is not data access related before said estimated response time elapses.

177. The processor chipset of Claim 173 further comprising a plurality of second data storage device control circuits each including a third I/O interface, wherein said port multiplier communicates with said third I/O interface of said second data storage device control circuits.

178. The processor chipset of Claim 165 wherein said I/O circuit is implemented by an I/O controller hub and further comprising:

a memory and graphics controller hub that communicates with said I/O controller hub and said processor.

179. The processor chipset of Claim 164 wherein said I/O circuit is implemented by a processor, memory, graphics and I/O chipset that communicates with said processor.

180. A processor chipset that communicates with a data storage device, comprising:

processor chipset input/output (I/O) means for providing an I/O interface to said processor chipset for at least one of serial, audio, basic input/output system (BIOS), local area network, mouse, and keyboard connections and that includes:

mapping means for mapping logical addresses to physical addresses;

data storage device controller (DSDC) means that communicates with said mapping means for controlling the data storage device; and

first I/O interface means for communicating with at least one of said DSDC means and said mapping means, wherein data to be stored on the data storage device and data storage device control signals including at least one of read/write arm position data and spindle control data are transmitted by said first I/O interface means to the data storage device.

181. The processor chipset of Claim 180 further comprising processing means that communicates with said processor chipset I/O means for performing at least one of data and control processing.

182. The processor chipset of Claim 181 further comprising:

system bus means that communicates with said processing means for transferring data;

peripheral component interconnect (PCI) bus means that communicates with said processing means for providing an interface to an expansion card slot; and

a Northbridge chipset that communicates with said processing means over said system bus means,

wherein said I/O means is implemented by a Southbridge chipset that communicates with said PCI bus means.

183. The processor chipset of Claim 180 wherein said processor chipset communicates with a data storage device control circuit that includes a second I/O interface means and at least one of spindle motor means for driving a spindle motor, read/write arm means for driving a read/write arm, and read channel means for driving a read channel, and wherein said first I/O interface means communicates with said second I/O interface means.

184. The processor chipset of Claim 183 wherein at least one of said DSDC means and said mapping means communicates data and control information to said read channel in-band over a serial link.

185. The processor chipset of Claim 183 wherein at least one of said DSDC means and said mapping means communicates data to said read channel in-band and control information to said read channel out-of-band.

186. The processor chipset of Claim 183 wherein the data storage device includes:

a data storage device platter;

a read/write arm;

a read/write head arranged on said read/write arm;

a spindle motor that communicates with said spindle motor means and that rotates said data storage device platter;

a read/write arm actuator that communicates with said read/write arm means and that adjusts a position of said read/write arm; and

a preamp means that communicates with said read channel means and said read/write head.

187. The processor chipset of Claim 180 wherein said mapping means at least one of maps logical addresses to physical addresses and monitors a location of a read/write head of the data storage device.

188. The processor chipset of Claim 183 wherein said first and second I/O interface means are serial ATA interfaces.

189. The processor chipset of Claim 181 wherein said processor chipset I/O means includes port multiplying means for providing multiple ports and that communicates with said first I/O interface means.

190. The processor chipset of Claim 181 wherein said processing means sends a data request that includes an expiration time to said mapping means, and wherein said mapping means cancels said data request if said DSDC means does not respond to said data request before said expiration time.

191. The processor chipset of Claim 181 wherein said processing means sends a data request to said mapping means, wherein said mapping means periodically receives at least one of head location and sector location status from said DSDC means, and wherein said mapping means sends an estimated response time for said data request to said processing means.

192. The processor chipset of Claim 191 wherein said processing means schedules at least one task that is not data access related before said estimated response time elapses.

193. The processor chipset of Claim 189 further comprising a plurality of second data storage device control circuits each including a third I/O interface means for providing an interface, wherein said port multiplying means communicates with said third I/O interface means of said second data storage device control circuits.

194. The processor chipset of Claim 181 wherein said processor chipset I/O means is implemented by an I/O controller hub and further comprising:

a memory and graphics controller hub that communicates with said processing means and said I/O controller hub.

195. The processor chipset of Claim 180 wherein said processor chipset I/O means is implemented by a processor, memory, graphics and I/O chipset.